Finisar

Product Specification

RoHS-6 Compliant
10Gb/s DWDM 80km Multi-Rate XFP Optical Transceiver
FTLX3811M3xx

PRODUCT FEATURES

- Supports 9.95Gb/s to 11.1Gb/s bit rates
- Hot-pluggable XFP footprint
- Maximum link length of 80km
- RoHS-6 compliant (lead-free)
- Temperature-stabilized DWDM-rated EML transmitter
- 100GHz ITU Grid, C-Band
- Duplex LC connector
- Power dissipation <3.5W
- Built-in digital diagnostic functions
- Temperature range: -5°C to 70°C

APPLICATIONS

- DWDM 10Gb/s SONET/SDH ITU-T G.698.1 S-D100S1-2D
- DWDM 10Gb/s SONET/SDH ITU-T G.709
- DWDM 80km 10G Ethernet
- DWDM 80km 10G Fibre Channel
- DWDM 80km 10G Ethernet with FEC

Finisar's 80km FTLX3811M3xx Small Form Factor 10Gb/s (XFP) transceivers comply with the current XFP Multi-Source Agreement (MSA) Specification[1]. They exceed the requirements for DWDM 10Gb/s SONET/SDH interfaces per ITU-T G.698.1 S-D100S1-2D, and support DWDM 10-Gigabit Ethernet, 10-Gigabit Fibre Channel, and 10-Gigabit Ethernet with FEC applications. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XFP MSA. The transceiver is RoHS compliant and lead free per Directive 2002/95/EC[3], and Finisar Application Note AN-2038[4].

PRODUCT SELECTION

FTLX3811M3xx

xx: 100GHz ITU-T channel (see next page)

Channel #	Product Code	Frequency (THz)	Center Wavelength (nm)
17*	FTLX3811M317	191.7	1563.86
18*	FTLX3811M318	191.8	1563.05
19*	FTLX3811M319	191.9	1562.23
20	FTLX3811M320	192.0	1561.42
21	FTLX3811M321	192.1	1560.61
22	FTLX3811M322	192.2	1559.79
23	FTLX3811M323	192.3	1558.98
24	FTLX3811M324	192.4	1558.17
25	FTLX3811M325	192.5	1557.36
26	FTLX3811M326	192.6	1556.55
27	FTLX3811M327	192.7	1555.75
28	FTLX3811M328	192.8	1554.94
29	FTLX3811M329	192.9	1554.13
30	FTLX3811M330	193.0	1553.33
31	FTLX3811M331	193.1	1552.52
32	FTLX3811M332	193.2	1551.72
33	FTLX3811M333	193.3	1550.92
34	FTLX3811M334	193.4	1550.12
35	FTLX3811M335	193.5	1549.32
36	FTLX3811M336	193.6	1548.51
37	FTLX3811M337	193.7	1547.72
38	FTLX3811M338	193.8	1546.92
39	FTLX3811M339	193.9	1546.12
40	FTLX3811M340	194.0	1545.32
41	FTLX3811M341	194.1	1544.53
42	FTLX3811M342	194.2	1543.73
43	FTLX3811M343	194.3	1542.94
44	FTLX3811M344	194.4	1542.14
45	FTLX3811M345	194.5	1541.35
46	FTLX3811M346	194.6	1540.56
47	FTLX3811M347	194.7	1539.77
48	FTLX3811M348	194.8	1538.98
49	FTLX3811M349	194.9	1538.19
50	FTLX3811M350	195.0	1537.40
51	FTLX3811M351	195.1	1536.61
52	FTLX3811M352	195.2	1535.82
53	FTLX3811M353	195.3	1535.04
54	FTLX3811M354	195.4	1534.25
55	FTLX3811M355	195.5	1533.47
56	FTLX3811M356	195.6	1532.68
57	FTLX3811M357	195.7	1531.90
58	FTLX3811M358	195.8	1531.12
59	FTLX3811M359	195.9	1530.33
60	FTLX3811M360	196.0	1529.55
61*	FTLX3811M361	196.1	1528.77

*****This channel is supported with limited availability -- Please contact Finisar for further details.

I. Pin Descriptions

Pin	Logic	Symbol	Name/Description	Ref.
1		GND	Module Ground	1
2		VEE5	Optional –5.2 Power Supply – **Not required**	
3	LVTTL-I	Mod-Desel	Module De-select; When held low allows the module to respond to 2-wire serial interface commands	
4	LVTTL-O	$\overline{\text{Interrupt}}$	Interrupt (bar); Indicates presence of an important condition which can be read over the serial 2-wire interface	2
5	LVTTL-I	TX_DIS	Transmitter Disable; Transmitter laser source turned off	
6		VCC5	+5 Power Supply	
7		GND	Module Ground	1
8		VCC3	+3.3V Power Supply	
9		VCC3	+3.3V Power Supply	
10	LVTTL-I	SCL	Serial 2-wire interface clock	2
11	LVTTL-I/O	SDA	Serial 2-wire interface data line	2
12	LVTTL-O	Mod_Abs	Module Absent; Indicates module is not present. Grounded in the module.	2
13	LVTTL-O	Mod_NR	Module Not Ready; Finisar defines it as a logical OR between RX_LOS and Loss of Lock in TX/RX.	2
14	LVTTL-O	RX_LOS	Receiver Loss of Signal indicator	2
15		GND	Module Ground	1
16		GND	Module Ground	1
17	CML-O	RD-	Receiver inverted data output	
18	CML-O	RD+	Receiver non-inverted data output	
19		GND	Module Ground	1
20		VCC2	+1.8V Power Supply	
21	LVTTL-I	P_Down/RST	Power Down; When high, places the module in the low power stand-by mode and on the falling edge of P_Down initiates a module reset	
			Reset; The falling edge initiates a complete reset of the module including the 2-wire serial interface, equivalent to a power cycle.	
22		VCC2	+1.8V Power Supply	
23		GND	Module Ground	1
24	PECL-I	RefCLK+	Reference Clock non-inverted input, AC coupled on the host board – **Not required**	
25	PECL-I	RefCLK-	Reference Clock inverted input, AC coupled on the host board – **Not required**	
26		GND	Module Ground	1
27		GND	Module Ground	1
28	CML-I	TD-	Transmitter inverted data input	
29	CML-I	TD+	Transmitter non-inverted data input	
30		GND	Module Ground	1

Notes:
1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; should be pulled up with 4.7k – 10kohms on host board to a voltage between 3.15V and 3.6V.

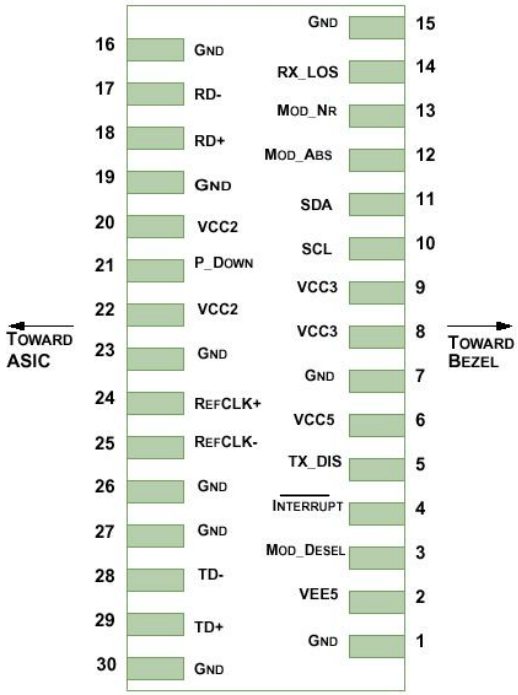


Diagram of Host Board Connector Block Pin Numbers and Names

II. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage #1	Vcc3	-0.5		4.0	V	
Maximum Supply Voltage #2	Vcc5	-0.5		6.0	V	
Maximum Supply Voltage #3	Vcc5	-0.5		2.0	V	
Storage Temperature	T_S	-40		85	°C	
Case Operating Temperature	T_{OP}	-5		70	°C	

III. Electrical Characteristics (T_{OP} = -5 to 70 °C, V_{CC5} = 4.75 to 5.25 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage #1	Vcc5	4.75		5.25	V	
Supply Voltage #2	Vcc3	3.13		3.46	V	
Supply Voltage #3	Vcc2	1.71		1.89	V	
Supply Current – Vcc5 supply	Icc5			350	mA	
Supply Current – Vcc3 supply	Icc3			400	mA	
Supply Current – Vcc2 supply	Icc2			750	mA	
Module total power	P			3.5	W	1
Transmitter						
Input differential impedance	R_{in}		100		Ω	2
Differential data input swing	Vin,pp	120		820	mV	
Transmit Disable Voltage	V_D	2.0		Vcc	V	3
Transmit Enable Voltage	V_{EN}	GND		GND+ 0.8	V	
Transmit Disable Assert Time				10	us	
Receiver						
Differential data output swing	Vout,pp	340	650	850	mV	4
Data output rise time	t_r			38	ps	5
Data output fall time	t_f			38	ps	5
LOS Fault	$V_{LOS\ fault}$	Vcc – 0.5		Vcc_{HOST}	V	6
LOS Normal	$V_{LOS\ norm}$	GND		GND+0.5	V	6
Power Supply Rejection	PSR	See Note 6 below				7
Reference Clock						
Clock differential input impedance	$Rclk_{in}$		100		Ω	
Reference Clock frequency	f0		Baud/64		MHz	
Differential clock input swing	Vclkin,pp	640		1600	mV	
Clock output rise/fall time	t_{rf}	200		1250	ps	5
Reference clock frequency tolerance	Df	-100		+100	PPM	

Notes:
1. Maximum total power value is specified across the full temperature and voltage range.
2. After internal AC coupling.
3. Or open circuit.
4. Into 100 ohms differential termination.
5. 20 – 80 %
6. Loss Of Signal is open collector to be pulled up with a 4.7k – 10kohm resistor to 3.15 – 3.6V. Logic 0 indicates normal operation; logic 1 indicates no signal detected.
7. Per Section 2.7.1. in the XFP MSA Specification[1].

IV. Optical Characteristics (EOL, T_{OP} = -5 to 70°C, V_{CC5} = 4.75 to 5.25 Volts)

Please note that the Transmitter of the FTLX3811M3xx becomes operational within 60 seconds of power-up. This is due to the time required for the EML to reach its optimum operating temperature.

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Output Opt. Pwr: 9/125 SMF	P_{OUT}	-1		+3	dBm	
Optical Extinction Ratio	ER	8.2			dB	
Center Wavelength Spacing			100		GHz	1
Transmitter Center Wavelength – End Of Life	λc	X-100	X	X+100	pm	2
Transmitter Center Wavelength – Beginning Of Life	λc	X-25	X	X+25	pm	2
Sidemode Supression ratio	SSR_{min}	30			dB	
Tx Jitter Generation (peak-to-peak)	Tx_j			0.1	UI	3
Tx Jitter Generation (RMS)	Tx_{jRMS}			0.01	UI	4
Relative Intensity Noise	RIN			-130	dB/Hz	
Receiver						
Receiver Sensitivity @ 9.95Gb/s	R_{SENS1}			-24	dBm	5,6
Receiver Sensitivity @ 11.1Gb/s	R_{SENS2}			-22	dBm	5
Maximum Input Power	P_{MAX}	-7			dBm	
Optical Center Wavelength	λ_C	1270		1600	nm	
Receiver Reflectance	R_{rx}			-27	dB	
Path penalty at 1450 ps/nm @ 10.7Gb/s	DP_1			2.5	dB	7,8
Path penalty at 1300 ps/nm @ 11.1Gb/s	DP_2			2.5	dB	8
LOS De-Assert	LOS_D			-30	dBm	
LOS Assert	LOS_A	-37			dBm	
LOS Hysteresis		0.5			dB	

Notes:
1. Corresponds to approximately 0.8 nm.
2. X = Specified ITU Grid wavelength.
3. Measured with a host jitter of 50 mUI peak-to-peak.
4. Measured with a host jitter of 7 mUI RMS.
5. Measured at 1528-1600nm with worst ER; BER<10^{-12}; PRBS31.
6. Equivalent to –22.1 dBm OMA at ER = 9 dB.
7. Dispersion penalty should be measured in loopback on a 1450 ps/nm fiber link.
8. Measured at BER<10^{-6}; PRBS31.

V. General Specifications

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate	BR	9.95		11.1	Gb/s	1
Bit Error Ratio	BER			10^{-12}		2
Max. Supported Link Length	L_{MAX}		80		km	1

Notes:
1. SONET OC-192, 10G Ethernet, 10G Fibre Channel, SONET OC-192 with FEC, 10G Ethernet with FEC.
2. Tested with a 2^{31} – 1 PRBS @ 9.95Gb/s and 10.3Gb/s

VI. Environmental Specifications

Finisar XFP transceivers have an operating temperature range from -5°C to +70°C case temperature.

Parameter	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	-5		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VII. Regulatory Compliance

Finisar XFP transceivers are Class 1 Laser Products. They are certified per the following standards:

Feature	Agency	Standard	Certificate Number
Laser Eye Safety	FDA/CDRH	CDRH 21 CFR 1040 and Laser Notice 50	9210176-77
Laser Eye Safety	TÜV	EN 60825-1: 1994+A11:1996+A2:2001 IEC 60825-1: 1993+A1:1997+A2:2001 IEC 60825-2: 2000, Edition 2	72101686
Electrical Safety	TÜV	EN 60950	72101686
Electrical Safety	UL/CSA	CLASS 3862.07 CLASS 3862.87	2283290

Copies of the referenced certificates are available at Finisar Corporation upon request.

VIII. Digital Diagnostics Functions

As defined by the XFP MSA[1], Finisar XFP transceivers provide digital diagnostic functions via a 2-wire serial interface, which allows real-time access to the following operating parameters:

- Transceiver temperature
- Laser bias current
- Transmitted optical power
- Received optical power
- Transceiver supply voltage

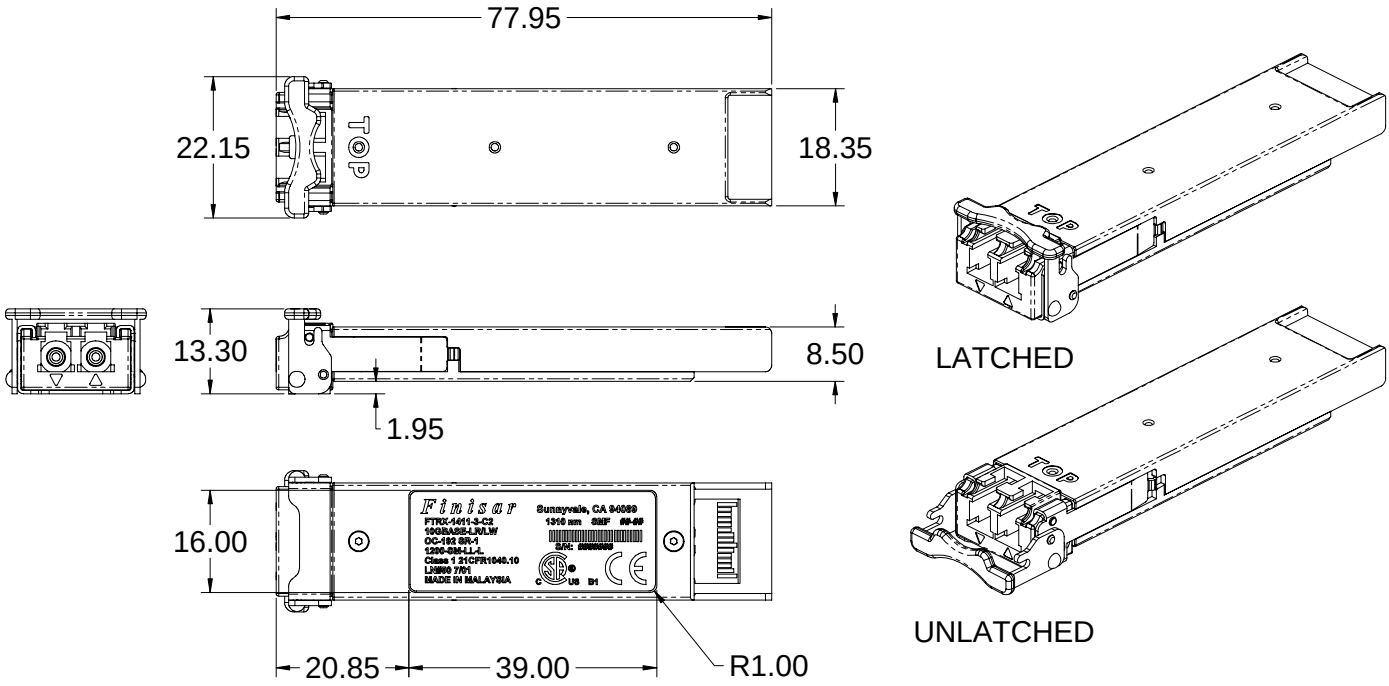
It also provides a sophisticated system of alarm and warning flags, which may be used to alert end-users when particular operating parameters are outside of a factory-set normal range.

The operating and diagnostics information is monitored and reported by a Digital Diagnostics Transceiver Controller (DDTC) inside the transceiver, which is accessed through the 2-wire serial interface. When the serial protocol is activated, the serial clock signal (SCL pin) is generated by the host. The positive edge clocks data into the XFP transceiver into those segments of its memory map that are not write-protected. The negative edge clocks data from the XFP transceiver. The serial data signal (SDA pin) is bi-directional for serial data transfer. The host uses SDA in conjunction with SCL to mark the start and end of serial protocol activation. The memories are organized as a series of 8-bit data words that can be addressed individually or sequentially. The 2-wire serial interface provides sequential or random access to the 8 bit parameters, addressed from 000h to the maximum address of the memory.

For more detailed information, including memory map definitions, please see the XFP MSA documentation[1].

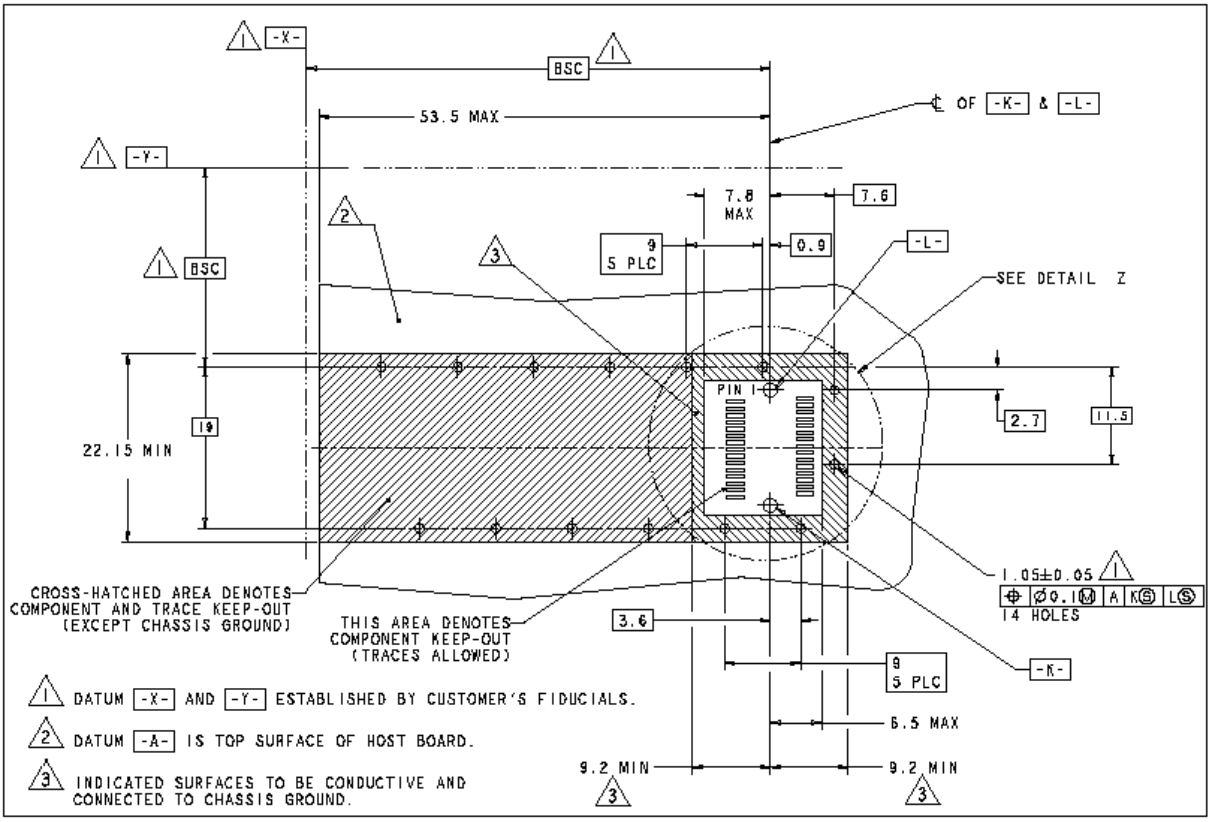
IX. Mechanical Specifications

Finisar's XFP transceivers are compliant with the dimensions defined by the XFP Multi-Sourcing Agreement (MSA).

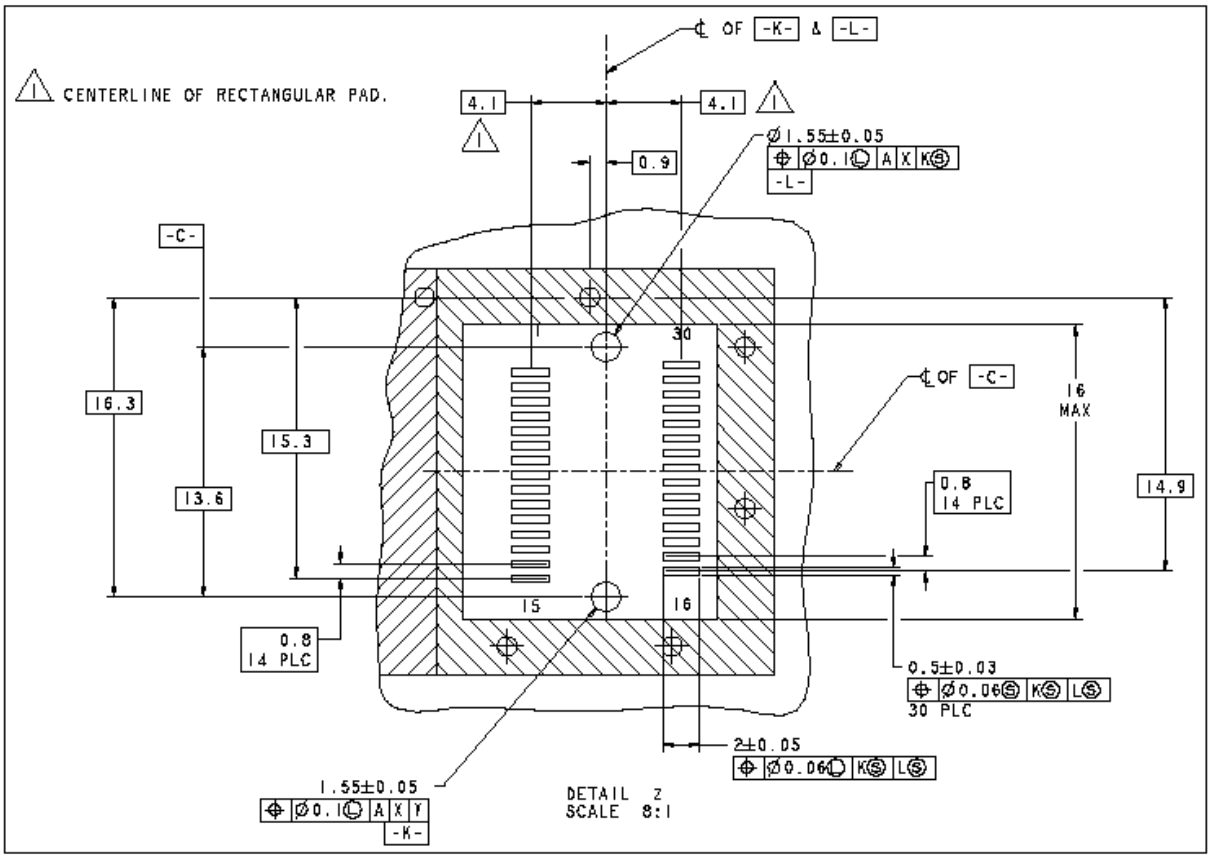


XFP Transceiver (dimensions are in mm)

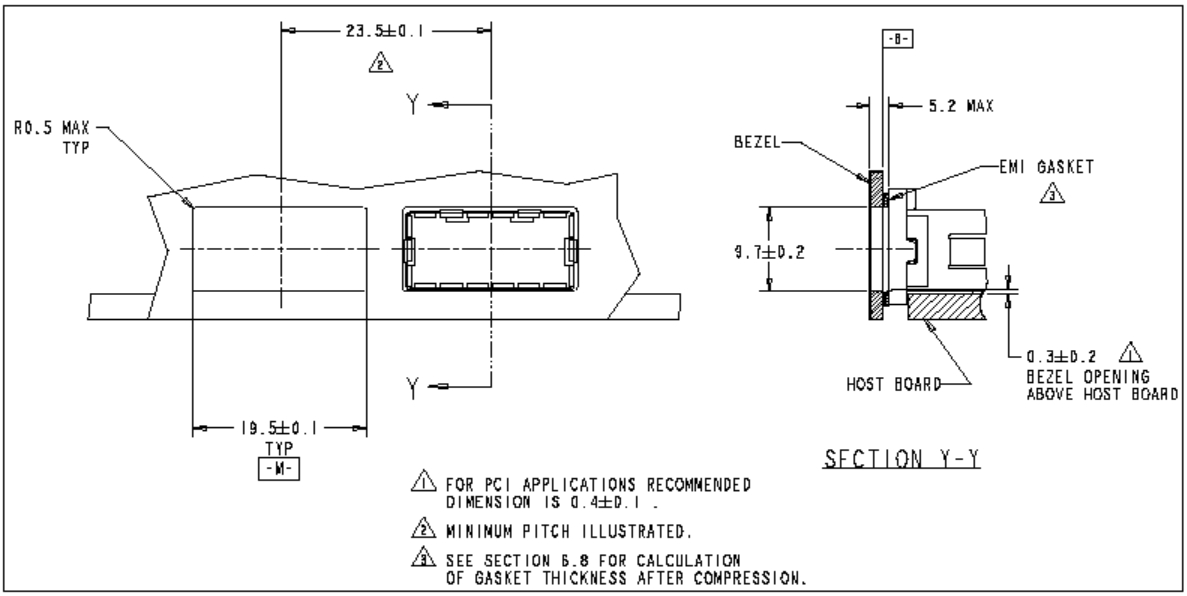
X. PCB Layout and Bezel Recommendations



XFP Host Board Mechanical Layout (dimensions are in mm)



XFP Detail Host Board Mechanical Layout (dimensions are in mm)



XFP Recommended Bezel Design (dimensions are in mm)

XI. References

1. 10 Gigabit Small Form Factor Pluggable Module (XFP) Multi-Source Agreement (MSA), Rev 4.5 – August 2005. Documentation is currently available at http://www.xfpmsa.org/
2. Application Note AN-2035: "Digital Diagnostic Monitoring Interface for XFP Optical Transceivers" – Finisar Corporation, December 2003
3. Directive 2002/95/EC of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment". January 27, 2003.
4. "Application Note AN-2038: Finisar Implementation Of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.

XII. Revision History

Revision	Date	Description
A	4/12/2006	• Document created.
A1	4/21/2006	• Updated photo. • Removed Finisar Confidential. • Updated Finisar Address.
A2	5/26/2006	• Change BOL wavelength specification.
B	10/25/2006	• Added Safety Certificate numbers. • Document released.
B1	12/18/2006	• Modified Min LOS Assert to -37dBm and Max LOS De-Assert to -30dBm • Modified path penalty to 2.5dB at BER<10^{-6} @ 10.7 Gb/s and 11.1Gb/s
B2	9/28/2007	• Updated note on channels.
C1	1/11/2011	• Updated Regulatory Compliance Information

XII. For More Information

Finisar Corporation
1389 Moffett Park Drive
Sunnyvale, CA 94089-1133
Tel. 1-408-548-1000
Fax 1-408-541-6138
sales@finisar.com
www.finisar.com